16U540 (Pages: 2) Name: ……..

Reg. No……

FIFTH SEMESTER B.C.A. DEGREE EXAMINATION, NOVEMBER 2018

(CUCBCSS-UG)

CC15U BCA5 B11 - COMPUTER ORGANIZATION AND ARCHITECTURE

(Computer Application - Core Course)

(2015 - Admission onwards)

Time: Three Hours Maximum: 80 Marks

Part A

Answer ***all*** questions. Each question carries 1 mark.

1. _____ is a group of bits that instruct the computer to perform a specific operation.
2. MISD stands for _____
3. _____ holds the address of the next instruction to be read from memory after the current instruction is executed.
4. A micro-program is a sequence of _____
5. _____ transmission can send and receive data in both directions simultaneously.
6. _____ memory is used to increase the speed of processing.
7. A pipeline register is a _____
8. When CPU refers to memory and finds the word in cache, it is said to produce _____
9. _____ is a set of rules that are followed by interconnecting computers to ensure orderly transfer of information.
10. _____ memory is a concept that permits the user to construct large programs equal to the totality of auxiliary memory.

(10 x 1 = 10 Marks)

Part B

Answer ***all*** questions. Each question carries 2 marks.

11. Explain instruction cycle of a basic computer.
12. Explain the working of a cache memory.
13. Write micro instruction format of a basic computer.
14. Explain cycle stealing mechanism.
15. Define data dependency in instruction pipeline.

(5 x 2 = 10 Marks)

Part C

Answer any ***five*** questions. Each question carries 4 marks.

16. Write a detailed note on different computer registers.

17. Demonstrate interrupt cycle.
18. Write a multiplication algorithm for multiplying binary instruction in signed 2's complement representation.
19. Explain DMA data transfer technique.
20. Explain the need and mechanism of memory interleaving.
21. Describe an array processor.
22. With the help of a block diagram explain general register organization.
23. Explain the use of associative memory.

(5 x 4 = 20 Marks)

Part D

Answer any ***five*** questions. Each question carries 8 marks.

24. What is the difference between a direct and an indirect address instruction? How do each type of instruction bring an operand into a processor register?
25. Explain address sequencing mechanism using control memory.
26. Explain stack organization.
27. Explain any two auxiliary memory devices.
28. Explain programmed I/O and interrupt I/O.
29. Explain arithmetic pipeline for floating point addition and subtraction.
30. What are RAM and ROM chips? How RAM and ROM chips are connected to CPU?
31. Explain vector processing in detail.

(5 x 8 = 40 Marks)

****