18U557 (Pages: 2) Name: ……..……..

Reg. No…….

FIFTH SEMESTER B.Sc. DEGREE EXAMINATION, NOVEMBER 2020

(CUCBCSS-UG)

(Regular/Supplementary/Improvement)

CC17U BCS5 B07 - COMPUTER ORGANIZATION AND ARCHITECTURE

(Computer Science – Core Course)

(2017 Admission onwards)

Time: Three Hours Maximum: 80 Marks

PART A

Answer ***all*** questions. Each question carries 1 mark

1. Define Handshaking.
2. Define DMA.
3. What is Nibble?
4. Differentiate between T Flip flop and D flip flop'.
5. Define MBR.
6. What is Accumulator?
7. Define Cache memory.
8. Give two examples of page replacement policy.
9. Differentiate between RAM and ROM.
10. What do you understand by immediate addressing mode?

(10 x 1 = 10 Marks)

PART B

Answer ***all*** questions. Each question carries 3 marks.

11. Explain Memory reference instructions.
12. What is direct mapping?
13. Draw the block diagram of Associate memory and explain.
14. Define bootstrap loader.
15. Differentiate between hardwired and micro programmed control.

(5 x 3 = 15 Marks)

PART C

Answer any ***five*** questions. Each question carries 5 marks.

16. Explain addressing mode with examples.
17. Write a brief note on:

    a. Memory hierarchy b. Isolated VS memory mapped i/o.

18. Explain the phases of instruction cycle.

19. Draw and explain the block diagram of an asynchronous communication interface.

20. Explain Daisy chaining priority interrupt.

21. Explain Shift registers.

22. Explain different types of Counters.

23. Compare and contrast SR, JK, Master-slave JK, D, T flip-flop.

(5 x 5 = 25 Marks)

PART D

Answer any ***three*** questions. Each question carries 10 marks.

24. Explain the DMA Structure and its working.

25. Explain the concept of Adders and Subtractor.

26. Explain about various Logic gates.

27. Write a note on Asynchronous data transfer.

28. Describe cache memory and explain different types of mapping procedures.

(3 x 10 = 30 Marks)

****