19U567S (Pages: 2) Name: ……..……

Reg. No: ……..

FIFTH SEMESTER B.C.A. DEGREE EXAMINATION, NOVEMBER 2021

(CUCBCSS-UG)

CC15U BCA5 B11 - COMPUTER ORGANIZATION AND ARCHITECTURE

(Core Course)

(2015, 2016 Admissions - Supplementary)

Time: Three Hours Maximum: 80 Marks

Part A

Answer ***all*** questions. Each question carries 1 mark

1. Cache memory works on the principle of --------
2. ADD X, Y is an example for --------
3. When CPU refers to memory and finds the word in cache, it is said to produce --------
4. A micro-program is a sequence of --------
5. The CPU register used for ALU operation is --------
6. -------- holds the address of the next instruction to be read from memory after the current instruction is executed.
7. The opcode specifies ---------
8. MISD stands for --------
9. Interrupts initiated by instructions are called --------
10. Cache memory acts between -------- and --------

(10 × 1 = 10 Marks)

Part B

Answer ***all*** questions. Each question carries 2 marks.

11. Explain working of a cache memory.
12. Define Interrupt cycle.
13. Define handshaking.
14. What do you mean by virtual memory?
15. Write the micro-instruction format of a basic computer.

(5 × 2 = 10 Marks)

Part C

Answer any ***five*** questions. Each question carries 4 marks.

16. Write a note on Stack organization.
17. Differentiate between CISC and RISC.
18. What are memory reference instructions?

19. Explain the design of accumulator logic.
20. Write a note on classification of ROM.
21. Explain daisy chaining priority interrupt.
22. Write a detailed note on different computer registers.
23. Explain the use of associative memory.

(5 × 4 = 20 Marks)

Part D

Answer any ***five*** questions. Each question carries 8 marks.

24. Write a note on DMA.
25. Explain the functional units of a computer.
26. Explain memory hierarchy.
27. Briefly explain the concepts of pipelining.
28. Explain data transfer and manipulation instructions.
29. Explain the condition and solution for cache coherence problem.
30. Explain address sequencing mechanism used in control memory.
31. Explain programmed I/O and Interrupt initiated I/O.

(5 × 8 = 40 Marks)

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