15U532 (Pages:2) Name: ……..

Reg. No…….

FIFTH SEMESTER B.Sc. DEGREE EXAMINATION, OCTOBER 2017

(CUCBCSS-UG)

CC15U BCS5 B08-COMPUTER ORGANIZATION AND ARCHITECTURE

(Computer Science – Core Course)

(2015-Admission Regular)

Time: Three Hours Maximum: 80 Marks

PART A

Answer ***all*** questions. Each question carries 1 mark

1. Define effective address
2. Define accumulator
3. Define cache memory.
4. Define latency.
5. Define auxiliary memory
6. Define MMU
7. Differentiate between hit and miss.
8. Define DMA
9. Explain cache coherence
10. Differentiate between MIMD and MISD

(10x1=10 Marks)

PART B

Answer ***all*** questions. Each question carries 2 marks

11. Explain about computer registers.
12. Explain addressing modes.
13. Define pipeline.
14. Define handshaking.
15. Define vector processor.

(5x2=10 Marks)

PART C

Answer any ***five*** questions. Each question carries 4 marks

16. What is instruction sequencing? Explain?
17. Explain the design of accumulator logic?
18. Explain booth algorithm for multiplication?

19. What are the memory reference instructions?
20. Explain the design of control unit?
21. What is locality of reference?
22. Explain about I/O processors?
23. Explain about asynchronous transfer?

(5x4=20 Marks)

PART D

Answer any ***five*** questions. Each question carries 8 marks

24. Explain the design of Basic computer?
25. Explain instruction cycle?
26. Explain the different types of instructions in basic computer design?
27. Explain is Memory hierarchy?
28. What is stack organization?
29. Briefly explain the concepts of pipelining
30. What are interrupts? Explain how priority interrupts are serviced?
31. Describe about parallel computers?

(5x8=40 Marks)

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