17U558A (Pages: 2) Name: ……..

Reg. No……...…….

FIFTH SEMESTER B.Sc. DEGREE EXAMINATION, NOVEMBER 2019

(Supplementary/Improvement)

(CUCBCSS-UG)

CC15U BCS5 B08 - COMPUTER ORGANIZATION AND ARCHITECTURE

(Computer Science – Core Course)

(2015 & 2016 Admissions)

Time: Three Hours Maximum: 80 Marks

PART A

Answer ***all*** questions. Each question carries 1 mark.

1. Define program counter.
2. What is the purpose of stack pointer?
3. Write an example for immediate address mode.
4. Name the data structure used to store the return address of subroutine call.
5. Define hit ratio?
6. What do you mean by cycle stealing?
7. What is handshaking?
8. Expand MIMD.
9. What is pipelining?
10. Expand NUMA.

(10 x 1 = 10 Marks)

PART B

Answer ***all*** questions. Each question carries 2 marks.

11. What is microprogram sequencer?
12. Convert infix to reverse polish notation: (A * B - (C - D)) * (E - F)
13. Draw memory hierarchy.
14. Define control memory and control address register.
15. What is cache coherence problem?

(5 x 2 = 10 Marks)

PART C

Answer any ***five*** questions. Each question carries 4 marks.

16. Explain general register organization.
17. Differentiate between hard wired and microprogrammed control unit.
18. Draw the flow chart for interrupt cycle.

19. With the help of an example explain direct and indirect addressing modes.
20. Compare Magnetic tape and Magnetic disks.
21. Short note on Daisy chaining priority.
22. Draw the flow chart for CPU-IOP communication.
23. Compare arithmetic pipeline with instruction pipeline.

(5 x 4 = 20 Marks)

PART D

Answer any ***five*** questions. Each question carries 8 marks.

24. Explain the different phases of an instruction cycle.
25. Illustrate the design of control unit.
26. Explain stack organization.
27. Explain the Booth's multiplication algorithm.
28. Describe the various mapping techniques used with cache memory.
29. Explain DMA controller in detail.
30. Describe Flynn’s classification of parallel computers.
31. Write a note on:

    1) Vector processing 2) Asynchonous data transfer

(5 x 8 = 40 Marks)

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