18U567 (Pages: 2) Name: ……..

Reg. No……...…….

FIFTH SEMESTER B.C.A. DEGREE EXAMINATION, NOVEMBER 2020

(CUCBCSS-UG)

(Supplementary/Improvement)

CC15U BCA5 B11 - COMPUTER ORGANIZATION AND ARCHITECTURE

(Computer Application - Core Course)

(2015, 2016 Admissions)

Time: Three Hours Maximum: 80 Marks

Part A

Answer ***all*** questions. Each question carries 1 mark.

1. _____ addressing mode is most suitable to change the normal sequence of execution of instructions.
2. _____ is the first process in instruction execution.
3. Write the principle of working of cache memory.
4. _____ register keeps track of the instructions stored in program stored in memory.
5. A floating point number that has a O in the MSB of mantissa is said to have _____
6. Which register is used to keep track of when the program was last accessed?
7. What is strobe signal?
8. Which register is cleared in a program using Sub routine call instruction?
9. What is Access time?
10. What is vectored interrupt?

(10 × 1 = 10 Marks)

Part B

Answer ***all*** questions. Each question carries 2 marks.

11. Define a multi programmed control unit.
12. Define hit and miss. What is meant by hit ratio?
13. Differentiate between RAM and ROM.
14. What are the advantages of interrupt?
15. What is pipelining?

(5 × 2 = 10 Marks)

Part C

Answer any ***five*** questions. Each question carries 4 marks.

16. Draw a flowchart to explain instruction cycle.
17. Explain Asynchronous data transfer.
18. Discuss in detail about cache coherence.

19. Write short note on Virtual Memory.
20. Give a brief description about addition and subtraction algorithms.
21. Explain about different types of Auxiliary Memories.
22. Write a short note on Direct Memory Access.
23. Distinguish between CISC and RISC.

(5 × 4 = 20 Marks)

Part D

Answer any ***five*** questions. Each question carries 8 marks.

24. Describe in detail about magnetic and optical storage devices.
25. Explain about general register organization of processor.
26. Explain about Cache Memory.
27. Describe about IO controllers.
28. Explain different types of hazards that occur in a pipeline.
29. Describe in detail about IOP organization.
30. Describe in detail about Stack Organization of processor.
31. Explain about vector processing and vector processors.

(5 × 8 = 40 Marks)

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