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# FIRST SEMESTER M.Sc. DEGREE EXAMINATION, NOVEMBER 2023 

(CBCSS - PG)
(Regular/Supplementary/Improvement)
CC19P PHY1 C04-ELECTRONICS
(Physics)
(2019 Admission onwards)
Time : 3 Hours
Maximum : 30 Weightage

## Section A

Answer all questions. Each question carries 1 weightage.

1. Explain the working of FET as a VVR.
2. Give a short note on Complemertary MOSFET (CMOS) arrangement.
3. What are direct and indirect bandgap semiconductors? How can we increase the quantum efficiency of an indirect band gap material?
4. What is a double hetero junction laser? How is optical confinement achieved in it?
5. Explain difference mode and common mode gains.
6. Explain input offset current and input bias current in Op-Amp.
7. Explain the basic principle of an Op - Amp comparator.
8. Explain the function and working of a shift register.
$(8 \times 1=8$ Weightage $)$

## Section B

Answer any two questions. Each question carries 5 weightage.
9. Draw the circuit of a common source amplifier with load resistor $R_{d}$ in the drain circuit and an additional resistor $\mathrm{R}_{\mathrm{S}}$ in the source to ground circuit. Draw the Thevenin's equivalent circuit looking into the drain. Derive the expressions for voltage gain.
10. What is a tunnel diode? Explain the principle of working of a tunnel diode, giving its characteristics.
11. Describe the working of op amp based a) Astable multivibrator and b) Schmitt trigger.
12. With the help of a block diagram of an 8085 microprocessor, explain its operations.
$(2 \times 5=10$ Weightage $)$

## Section C

Answer any four questions. Each question carries 3 weightage.
13. Starting from the definitions of $g_{m}$ and $r_{d}$ show that if two identical FETs are connected in parallel, $g_{m}$ is doubled and $r_{d}$ is halved where $\mu$ remains unchanged.
14. Give the working principles of photoconductor and photodiode.
15. Discuss dominant pole compensation in Op-Amp.
16. Derive an expression for the output voltage of an inverting summing amplifier.
17. Design a second order high pass filter for a cut off frequency 5 kHz ( take $\mathrm{C}=0.01 \mu \mathrm{f}$ ).
18. A truth table has high outputs for $0001,0101,1010,1011,1100,1101$ and low for all other inputs. Use karnaugh map simplification and draw the simplified logic circuit.
19. Design a $\mathrm{D} / \mathrm{A}$ converter with R and 2 R resistor which converts a three input signal ranging from 000 to 111 .

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(4 \times 3=12 \text { Weightage })
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