19P109   (Pages: 2)   Name: ………..………….

Reg. No……..………....

FIRST SEMESTER M.Sc. DEGREE EXAMINATION, NOVEMBER 2019

(CUCSS PG)

CC19P PHY1 C04 – ELECTRONICS

(Physics)

(2019 Admission Regular)

Time: Three Hours   Maximum : 30 Weightage

Part A
Answer *all* questions. Each question carries 1 weightage.

1. Write a note on digital MOSFET circuit.

2. Explain how the FET acts as a VVR.

3. Draw the characteristic curve of tunnel diode.

4. What is the Butterworth response?

5. Draw the block diagram of master slave JK flip flop.

6. What do you mean by min-term and max-term? Illustrate.

7. Distinguish between static and dynamic RAM.

8. Outline the working of charge coupled devices.

(8 × 1 = 8 Weightage)

Part B
Answer any *two* questions. Each question carries 5 weightage.

9. Discuss the operating principle of Solar cell stating clearly what is meant by short circuit current, fill factor and efficiency.

10. Discuss the features of dominant pole, pole zero and lead compensation.

11. Discuss with theory the working of first order and second order low pass filters.

12. With the help of block diagram of an 8085 microprocessor, explain its operation.

(2 × 5 = 10 Weightage)

Part C
Answer any *four* questions. Each question carries 3 weightage.

13. If V_g of FET amplifier changes from -4.2 V to -4.1 V, the drain current changes from 1 mA to 3 mA. Find the voltage amplification if the load resistance R_d = 5 kΩ. Assume $r_d >> R_d$

14. Starting from the definitions of g_m and r_d show that if two identical FETs are connected in parallel, g_m is doubled and r_d is halved where μ remains unchanged.

15. Calculate the open circuit voltage and the output power at a voltage of 30V for solar cells which have I_L = 110 mA, I_S = 1 nA, area = 4 cm^2, T = 290 K

16. With necessary theory, design a notch filter of frequency 70 Hz

17. Design a second order high pass filter for a cut off frequency 5 kHz (C = 0 .01μF)

18. Draw the truth table of the system which has high outputs when the equivalent decimal inputs are 1, 2, 3, 7, 8, 9, 10 and 13 and low for all other inputs. Draw the Karnaugh map for the truth table and obtain the simplified Boolean equation of the system.

19. Design a six input D\A converter with a R-2R network.

(4 × 3 = 12 Weightage)

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