25P162 (Pages: 2) Name: .....

Reg.No: .....

FIRST SEMESTER M.Sc. DEGREE EXAMINATION, NOVEMBER 2025

(CBCSS - PG)

(Regular/Supplementary/Improvement)

CC19PCSS1C05 - COMPUTER ORGANIZATION AND ARCHITECTURE

(Computer Science)

(2019 Admission onwards)

Time : 3 Hours Maximum : 30 Weightage

Part-A

Answer any ***four*** questions. Each question carries 2 weightage.

1. Compare and contrast sequential circiut and combinational circuits.
2. Briefly explain Demultiplexer with diagram.
3. Distinguish between direct and indirect addressing modes with examples.
4. Differentiate RISC and CISC.
5. Write a detailed note on memory reference instructions.
6. Explain signed 2's complement addition and substraction operations.
7. Describe DMA controller.

(4 × 2 = 8 Weightage)

Part-B

Answer any ***four*** questions. Each question carries 3 weightage.

8. Explain binary arithmetic rules and examples in detail.
9. Illustrate the design of control unit with suitable diagram and explain its types.
10. What is array multiplier? Explain with an example.
11. What is mapping in cache memory? Explain any two mapping techniquesin detail.
12. Give comparison between memory mapped I/O and I/O mapped I/O.
13. Explain various modes of data transfer between CPU and peripheral devices.
14. Describe 8051 micro controller with suitable diagram.

(4 × 3 = 12 Weightage)

Part-C

Answer any ***two*** questions. Each question carries 5 weightage.

15. Minimize using Kmap a) A'B'C'+AB'C+A'BC+ABC' b) AC[B'+B(B+C')] c) DEF'+D'EF'+D'E'F'. Find the corresponding POS expression.

16. Explain the multiplication using Booth algorithm.

17. Explain the virtual memory translation and TLB with necessary diagram.

18. Explain 8051 microcontoller internal architecture and working with help of diagram.

(2 × 5 = 10 Weightage)

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