

17U557

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Name:

Reg. No.....

FIFTH SEMESTER B.Sc. DEGREE EXAMINATION, NOVEMBER 2019

(CUCBCSS-UG)

CC17U BCS5 B07- COMPUTER ORGANIZATION AND ARCHITECTURE

(Computer Science – Core Course)

(2017 Admission Regular)

Time: Three Hours

Maximum: 80 Marks

PART A

Answer *all* questions. Each question carries 1 mark.

1. Give the logic symbol for XOR gate.
2. Identify the gates needed to implement $A + \bar{B}$
3. What is a latch?
4. If the input bits of a half adder are $x=1, y=1$, determine its sum and carry.
5. How many select lines will a 16 to 1 multiplexer have?
6. What is the purpose of stack pointer?
7. Define instruction cycle.
8. Draw the format of control word.
9. What is handshaking?
10. What do you mean by cycle stealing?

(10 x 1 = 10 Marks)

PART B

Answer *all* questions. Each question carries 3 marks.

11. Draw the logic diagram and truth table of a half adder.
12. Write the applications of a decoder.
13. Explain memory hierarchy.
14. Define control memory and control address register.
15. Draw the flow chart for interrupt cycle.

(5 x 3 = 15 Marks)

PART C

Answer any *five* questions. Each question carries 5 marks.

16. What are the basic operations of a flip flop? What are edge triggered flip flops?
17. How do you construct
 - a. D flip flop from SR flip flop
 - b. T flip flop from JK flip flop.
18. What is ring counter? Write its merits and demerits.

19. Compare the mode of operations of all types of shift registers.
20. Explain general register organization.
21. Distinguish between direct and indirect addressing modes with example.
22. Differentiate between hard wired and microprogrammed control unit.
23. Explain the modes of transfer.

(5 x 5 = 25 Marks)

PART D

Answer any *three* questions. Each question carries 10 marks.

24. Why NAND is preferred over NOR as a universal gate? Redesign NOT, OR and NOR using NAND.
25. Explain in detail the working of up/down counters.
26. Illustrate the design of control unit.
27. Explain stack organization in detail.
28. Describe the various mapping techniques used with cache memory.

(3 x 10 = 30 Marks)
